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POWER OPTIMIZATION OF VLSI CIRCUITS USING WIRING/INTERCONNECT GEOMETRY

As the transistor size is scaling down the interconnect becomes more important in integrated circuit design, for instance, the delay caused by the interconnect is larger than the of gate in 0.13um technology. The overall delay is proportional to RC of the wire reducing the width of the wire means increasing the resistance due to decrease in conductor in cross-sectional area. Increasing the width of wire means increasing capacitance since the conductor space increases. Trade-off must be done to reduce delay.

The rapid increase in the number of wiring layers due to improved planarization and metallization techniques permits spatial resources to be traded for improved performance yield ,power dissipation and propagation delay are all sensitive to the selection of the pitch and width of wires in each layer. The use of Pareto genetic algorithms is to explore the extent of multi-objective optimal surfaces .The tradeoffs between power-dissipation and cycle time for a bench mark net list are examined as a function of in-geometry for seven layer-interconnect.

As interconnect geometry that is neither optimal in terms of its clock rate or its power dissipation cannot itself be optimal. However it is possible to define design solutions ,which are optimal in th tradeoff between these two objectives: such solutions are referred to Pareto optimal. These quantities are dependent on interconnect geometry and on the specific details of the net list and its layout .With an estimate for wire length distribution in each layer ,layer dependent performance objectives can be calculated .The calculation of the circuit length distribution is usually tackled in 2 stages :the enumeration of the number of two terminal net placement sites of length for a given floor plan.

The occupation of these possible placement sites is determined by power-law occupancy probability .The length distribution within each wiring layer may be estimated using a simple routing model. The overall wire length distribution is used as an iterative algorithm ,which begins by calculating maximum wiring capacity in each layer.

The iterative algorithm allocates wires from first wiring layer ,shortest wires first until the available wiring capacity of the layer is needed. Then wires are allocated to the net highest layer and so in, until either all the wire are allocated or the available capacity of the highest layer is exceeded ,in which case the circuit is unconstructable. This process results in an estimate for the distribution of wire length in each layer.

Unlike conventional optimization methods like the simplex method or gradient based techniques the y are stochastic in nature and operate on entire populations of coed versions of candidate solutions in parallel. Genetic algorithms are especially attractive for complicated engineering design problems. Before applying a GA to design problem, an

objective function and a design parameter representation must be chosen. The objective function is a function of the design parameters that measures the goodness of a given design. This thus represents the quantity to be maximized or minimized by the GA. In the present case of a on-chop wiring design ,the objective function value may be clock speed (maximization) or power dissipation(minimization).

Given only the net list for the chip design ,the method can produce a curve in a two-dimensional space representing the best tradeoffs between two conflicting design goals. Pareto fronts and sample designs produce for two combinations of the design criterion listed above. The results clearly illustrate the importance of the technique by showing the vast untapped possibilities available in chip wiring design.