Hardware Realization of the Video Encoder Using an Efficient 3-D DCT Algorithm

Ganapathi Hegde, Harikrishna H, Shikha Tripathi, P. R. Vaya

Abstract:

This paper presents hardware architecture for a video encoder which employs 3-D discrete cosine transform (3-D DCT) algorithm. The algorithm adapts entropy reduction technique of DCT and does not require the second transpose memory in construction of hardware architecture. Hardware implementation enhances the compression performance of the video data and provides improved performance in power, area, and speed. The proposed hardware architecture for 3-D DCT and video encoder are described using Verilog hardware description language (HDL) and simulated using Modelsim SE 6.5. It is mapped on 90nm technology standard cell library using Synopsys design Compiler and layout is done using Synopsys back end IC and DC Compiler.