2009 Second International Conference on Computer and Electrical Engineering

Low Power Consumption Coarse Grained Reconfigurable Adder

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***Abstract*---Reconfigurable architecture gives the advantage of both high performance and high flexibility. However power consumption is also an important criterion which determines the efficiency of the reconfigurable architecture to be used in data intensive applications like cryptography, multimedia and signal processing. This paper analyzes a coarse grained reconfigurable adder which can be dynamically reconfigured with respect to bitwidth of operands. Using multiplexers and appropriate control bits, part of the architecture may be powered-down according to the requirement, thereby saving power because of the inactive state of unused part. It is described in Verilog HDL and Synthesized on to Xilinx spartan-2 FPGA. Xilinx Xpower analyzer is used to find the power consumption. Experimental results of this design show the edge over existing design in terms of power consumption.**

I. INTRODUCTION

Reconfigurable devices are those in which functionality can be changed during execution. They are divided into fine grained Field Programmable Gate Arrays FPGAs and Coarse Grained Reconfigurable Architectures CGRAs. Any hardware can be implemented in any of the platforms like Application Specific Integrated Circuit ASIC, FPGA or CGRA. The choice of implementation platform is driven by multiple factors like performance needed, power consumption, flexibility, and development cost. FPGAs are highly flexible but have drawbacks because of low granularity in terms of increased power, area, and delay due to greater quantity of routing required per computation. However CGRAs provide word level reconfiguration whose performances is higher than FPGAs and are power efficient. ASICs are application specific, so its performance is very high and are least flexible. However CGRAs are preferred to ASICs because it combines high degree of flexibility with high performance. Reconfigurable platforms provide computational efficiency of direct logic implementations in ASIC . CGRAs can be configured by loading a complete specification of the function of each part of the devices at once [6]. Once configured the device runs in that configuration for some time before being reconfigured. So CGRAs provide ideal platform for implementation of any hardware.

II. POWER DISSIPATION

Power is considered as the most important constraint in any application. Energy is a critical non functional constraint in battery powered systems. Average power dissipation determines thermal profile of the chip, chip packaging, electron migration. There are two types of power dissipation in CMOS which are static dissipation and dynamic dissipation.

A. STATIC DISSIPATION

Static dissipation in CMOS devices is due to leakage current or other current drawn continuously from the power supply. The main cause of static dissipation is due to sub threshold leakage from V_{DD} to ground. It may also occur due to reverse bias leakage current between diffusion region and substrate. The static power dissipation is given by the product of device leakage current and the supply voltage. It usually occurs in pseudo nMOS gates where there is direct path between power and ground.

B. DYNAMIC DISSIPATION

Dynamic power is due to switching transient current and due to charging and discharging of load capacitances. The dynamic power dissipation is of more importance to us as this occurs mainly during switching activity. Dynamic short circuit power is due to direct current path from V_{DD} to ground during output switching. Dynamic switching power is due to charging and discharging of load capacitance. The dynamic power P_D is given by

$P_d=C_L V_{DD}^2 f_p$

C_L -- load capacitance

f_p -- frequency of switching

978-0-7695-3925-6/09 $26.00 © 2009 IEEE
DOI 10.1109/ICCEE.2009.195

III. POWER MANAGEMENT TECHNIQUES

Power management techniques are in use at various levels of abstraction like OS level, Software level, Architectural level, Circuit level or logic level and Technology level. Greater power saving opportunities are available at higher levels of abstraction because it offers greater accuracy of switching activity. At architectural level power reduction is achieved by using pipelining, redundancy, data encoding, reconfigurability and various other techniques. However in this paper we discuss reconfigurable logic for saving power by reducing the switching activity.

IV. RECONFIGURABLE ADDER DESIGN

The conventional 128 bit carry look ahead adder is shown in the Fig. 1. It directly adds two 128 bit numbers and outputs the value as sum. The 128 bit reconfigurable carry look ahead adder[2] design is shown in Fig. 2. The design has been modified for our analysis by adding three enable pins to control the operation of the design. The circuit is made up of two 32 bit adders, a 64 bit adder and three one bit carry registers. The design can support 5 modes of operation such as 32 bit single and double (D32), 64 bit single and double (D64) and 128 bit additions. To realize the various modes we use 5 control bits which are decoded into 8 control signals internally. The extra 3 signals are enable bits, which help in disabling a part of the design to bring in flexibility and reduced power consumption due to inactive state of the unused part. It has 3 multiplexers whose outputs are dynamically controlled by the different modes of operation.

Table I describes the different modes of operation and their corresponding enable pins and output of multiplexers. In a single 32 bit mode, one 32 bit adder is enabled (En1=1) and the other two adders are disabled by de asserting their respective enables (En2=En3=0). Reg3, Reg2 and Reg1 store the carry of respective adders. MUX1 outputs the carry R1 and gives it as input carry to the first 32 bit adder. In double 32 bit mode two 32 bit adders are enabled (En1=En2=1) and work independently, and 64 bit adder is disabled (En3=0). MUX1 outputs R1, the carry output of first adder and is fed back as carry input to the first adder. MUX2 outputs R2, the carry output of second adder, which goes in as carry input. In 64 bit mode two 32 bit adders are enabled (En1=En2=1), and 64 bit adder is disabled (En3=0). MUX1 outputs R2, the carry out of second 32 bit adder, and is fed back as carry input to the first 32 bit adder. MUX2 outputs the carry from first 32 bit adder $CI_{32s.}$ Rest of the modes namely D64, 128 and E128 use all the three adders (En1=En2=En3=1). Mode D 64 is for two 64 bit additions similar to mode D 32. Mode 128 is similar to modes 32 and 64 bit additions and the corresponding outputs of the multiplexers are mentioned in Table I.

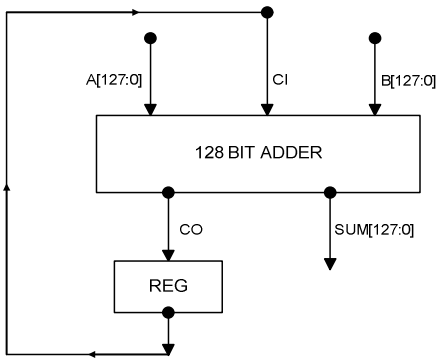

Fig. 1. 128 bit Conventional Adder

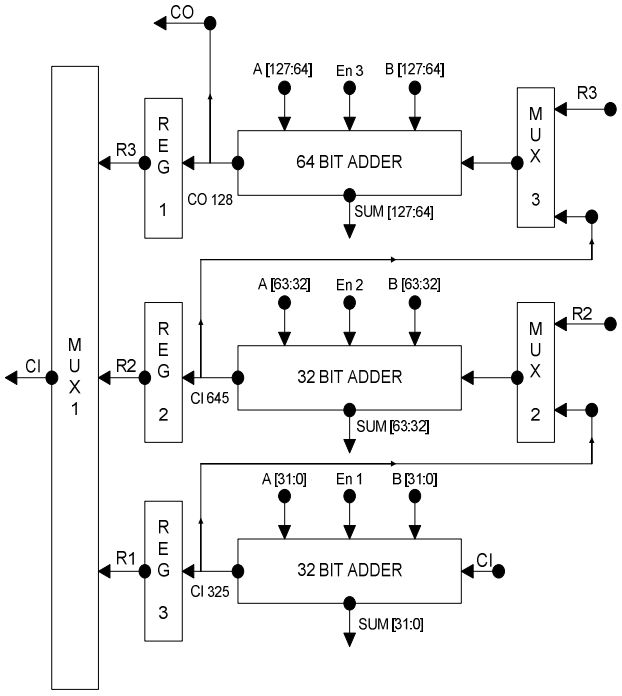

Fig. 2. 128 bit Reconfigurable Carry Look Ahead Adder

TABLE I

Table for different modes of 128 bit reconfigurable adder

Mode	Enable			MUX1 O/P	MUX2 O/P	MUX3 O/P
	En3	En2	En1			
32	0	0	1	R1	-	-
D 32	0	1	1	R1	R2	-
64	0	1	1	R2	CI_{32S}	-
D 64	1	1	1	R2	CI_{32S}	R3
128	1	1	1	R3	CI_{32S}	CI_{64S}

TABLE II

Table for Clock frequency at 100MHz and input toggle frequency at 50MHz.

Mode Toggle (in MHz)	Power Consumption (in W)		% Reduction In Power Consumption
	Conventional Adder	Reconfigurable Adder	
50	2.709	0.587	78.34
40	2.709	0.564	79.19
30	2.709	0.542	80
20	2.709	0.497	81.66
10	2.709	0.451	83.4
1	2.709	0.410	84.87

TABLE III

Table for Clock frequency at 50MHz and input toggle frequency at 25MHz.

Mode Toggle (in MHz)	Power Consumption (in W)		% Reduction In Power Consumption
	Conventional Adder	Reconfigurable Adder	
25	1.420	0.365	74.3
20	1.420	0.349	75.43
10	1.420	0.324	77.19
1	1.420	0.282	80.15

V. EXPERIMENTAL RESULTS

Both the circuits were described in Verilog HDL and simulated using ModelSim. Power analysis was done in Xilinx Xpower analyzer. Power is analyzed for different clock frequencies, in which the input pins and mode pins are toggled at different frequencies. The maximum frequency of the input signals can be half of that of the clock frequency. For example if the clock frequency is x (Hz) the inputs are toggled at a maximum of x/2 (Hz). The results are tabulated in the table II and III.

Table II describes the analysis in which input clock frequency is 100MHz. The input pins are toggled at 50MHz and the power consumption in Watt for both conventional and reconfigurable adder is recorded for different mode toggling frequency. For a particular input toggle frequency, power remains unchanged for the conventional adder, irrespective of mode toggle frequency because it does not support any modes which are mentioned in Table II. It also shows the worst case situation where the mode pins change at every clock edge. Table III describes the same operation in which all the values are exactly half i.e. input clock frequency is 50 MHz and input toggling frequency is 25MHz. If the mode toggle frequency is reduced below 1MHz, we find that the percentage reduction in power is almost the same as obtained for a mode toggle frequency of 1MHz.

Fig.3. shows the plot of mode frequency versus % power reduction for an input clock frequency of 100MHz. We can see that as the mode frequency decreases, the % power reduction increases, and has a maximum value of 84.87% for a mode toggling frequency of 1MHz.

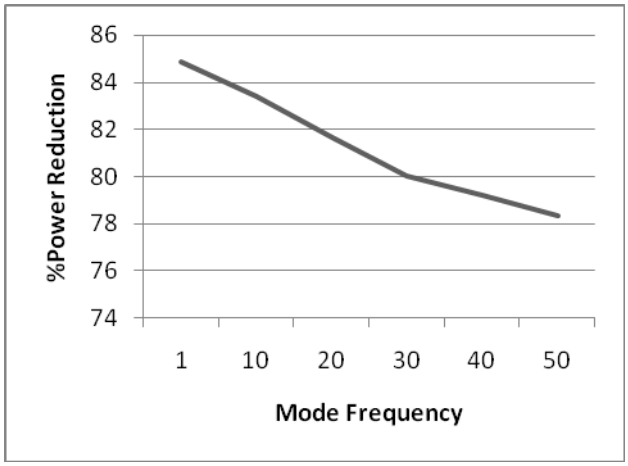

Fig. 3. % Power Reduction Vs Mode Frequency with input clock frequency at 100MHz

Fig.4. shows same for input clock frequency of 50MHz. As the mode frequency decreases, the % power reduction increases as in the previous case. Power reduction has a maximum value of 80.15% for a mode toggling frequency of 1MHz.

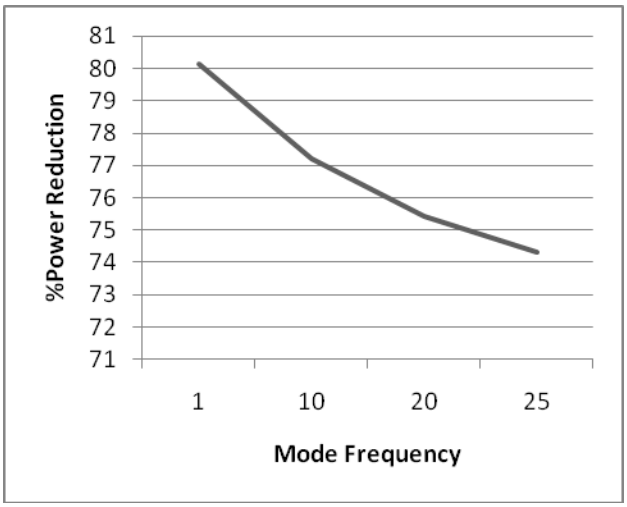

Fig. 4. Power Reduction Vs Mode Frequency with input clock frequency at 50MHz

VI. CONCLUSION

In this paper we have dynamically reconfigured a 128 bit adder. Both the designs were synthesized in Xilinx ISE 10.1 and power analysis was done in Xilinx Xpower analyzer. Power consumption was observed for varying clock frequencies and input signal toggling in both the designs and frequency-power graphs were plotted. From experimental results we get an average power consumption of 79.45% and a maximum of 84.87%. This proves that the modified design is more power efficient and is applicable to data intensive applications.

VII. FUTURE WORK

We plan to extend our work by reconfiguring functional parts of a processor which provides a suitable platform for cryptographic applications.

ACKNOWLEDGMENT

We bow down to Almighty for being the driving force behind us to do this work and would like to thank Amrita Vishwa Vidyapeetam for providing the necessary facilities in particular the access to Digital Library.

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